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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/400,508	09/20/99	ALLEE D	2000.000900

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EXAMINER	
CHO, J	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 09/26/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applic[illegible]s)
09/400,508	Allee
Examiner	**Group Art Unit**
James H. Cho	2819

☒ Responsive to communication(s) filed on *Sep 20, 1999*

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claim

☒ Claim(s) *1-9* is/are pending in the applicat

Of the above, claim(s) _____ is/are withdrawn from consideration

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-9* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☒ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

— SEE OFFICE ACTION ON THE FOLLOWING PAGES —

Claim Objections

1. Claims 1-9 are objected to because of minor informalities:

in claim 1, "the output" on line 7 appears to be --said output--, and "the voltage" on line 8 appears to be --said voltage--;

in claims 2-5 and 7-9, "A logic" on line 1 appears to be --the logic-- respectively;

in claim 2, "the voltage" on line 2 appears to be --said voltage--, and "the output" and "the transistor" on line 3 appears to be --said output-- and --said transistor-- respectively;

in claim 4, "the output" and "the voltage" on lines 1-2 appears to be --said output-- and --said voltage-- respectively;

in claim 5, "the output" and "the voltage" on line 2 appears to be --said output-- and --said voltage-- respectively;

in claim 6, "the output" and "the voltage" on lines 7-8 appears to be --said output-- and --said voltage-- respectively;

in claim 7, "the first", "the voltage", "the output", and "the intrinsic" on lines 2-3 appears to be --said voltage--, --said output--, and --said intrinsic-- respectively;

in claim 8, "the output" and "the voltage" on lines 1-2 appears to be --said output-- and --said voltage-- respectively;

in claim 9, "the output" and "the voltage" on line 2 appears to be --said output-- and --said voltage-- respectively.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

3. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Lee (US PAT. 6,078,194). Lee shows and teaches all the elements and means of the claimed invention of the claim 1:

Lee teaches a logic gate (see Fig. 4(a) and 4(b)), comprising: a low noise current source (see 32) coupled between a first terminal of a voltage supply (see Vcc) and an output terminal (see OUT in Fig. 1), the low noise current source being capable of delivering a preselected voltage signal to the output terminal having a magnitude responsive to a first control signal (see PEN) relatively independent of the magnitude of the voltage on the first terminal of the voltage supply, and at least one switching element (see 36 and 38) coupled between the output terminal and a second terminal (see VTT) of the voltage supply, the switching element being capable of coupling the output terminal to the second terminal of the voltage supply in response to receiving a control signal (see A or B).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (US PAT. 6,078,194).

Lee discloses the logic gate as set forth in claim 1 where the low noise current source includes a transistor (see 32) and a second transistor (see 34) whose gate is connected to the source serially coupled between the first terminal of the voltage supply and the output terminal, the transistor having a gate capable of receiving the first control signal, but does not discloses the second transistor being a resistor.

However, it is well known in the art that the second transistor is configured as a diode and the diode configured transistor is recognized as equivalent to a resistor in this environment. Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have replace the second transistor of Lee with a resistor for the purpose of reducing through current.

6. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (US PAT. 6,078,194) in view of Chang et al. (US PAT. 5,955,893).

Lee discloses the logic gate, as set forth in claim 1 but does not disclose the transistor is an intrinsic transistor.

However, Chang et al. discloses an intrinsic transistor (see 508 in Fig. 6) for the purpose of providing a transistor having a lower magnitude of threshold voltage.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to combine the transistor of Lee with the intrinsic transistor of Chang et al. because it would provide full voltage at the output terminal since the threshold voltage of the intrinsic transistor is lower than non-intrinsic transistor.

7. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (US PAT. 6,078,194) in view of Thompson et al. (US PAT. 3,651,334).

Lee discloses the logic gate, as set forth in claim 1 but does not disclose a capacitor coupled between the output terminal and the second terminal of the voltage supply.

However, Thompson et al. discloses a capacitor (see 28 in Fig. 1) coupled between the output terminal and the ground for the purpose of providing charging the output node.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to combine the logic gate of Lee with the capacitor of Thompson because it would provide a precharged voltage.

8. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (US PAT. 6,078,194) in view of Sundstrom (US PAT. 5,602,494).

Lee discloses the logic gate, as set forth in claim 1 but does not disclose at least one clamping diode coupled between the output terminal and the second terminal of the voltage supply.

However, Sundstrom discloses a clamping diode (see 142 in Fig. 2) coupled between the output terminal and a second terminal for the purpose of providing input protection.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to combine the logic gate of Lee with the clamping diode of Sundstrom because it would provide input protection from an external terminal.

9. Apparatus claims 6-9 are essentially the same in scope as rejected apparatus claims 1-5 and are rejected similarly.

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Yetter (US PAT. 5,389,835) discloses a vector logic method and dynamic mousetrap logic gate for a self-timed monotonic logic progression.

Wu et al. (US PAT. 4,777,389) discloses output buffer circuits for reducing ground bounce noise.

Ikawa et al. (US PAT. 4,639,621) discloses a gallium arsenide gate array integrated circuit including DCFL NAND gate.

Contact Information

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to ***James H. Cho*** whose telephone number is (703)306-5442. The examiner can normally be reached between the hours of 5:30 AM to 2:30 PM Monday thru Friday.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

James H. Cho

Patent Examiner, Art Unit 2819

September 21, 2000

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